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	APPLICANT Frederic Reblewski et al.	
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## U.S. PATENT DOCUMENTS

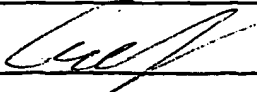
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE
A	5,363,319	11/1994	Okuda	—	—	
	5,574,388	11/1996	Barbier et al.	—	—	
	5,596,742	01/1997	Agarwal et al.	—	—	
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	5,920,712	07/1999	Kuijsten	—	—	

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION YES/NO
A	WO 94/06210	03/1994	PCT			
	WO 94/23389	10/1994	PCT			
	04-138569	05/1992	Japan			
	08-030653	02/1996	Japan			
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A	Babb et al., "Logic Emulation with Virtual Wires", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 16, No. 6, pgs. 609-626, June 1997.
	Translation of an Office Action of Japanese Patent Office, " from a Japanese counterpart application, 7 pages, July 2, 2002.
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	Berger, "Teramac HW Simulator System External Reference Specification," November 7, 1991, Revision 1.1, pp. 3-37.
	Snider et al., "The PLASMA Chip Specification," August 1, 1995, pp. 1-124.
	Snider et al., "The Teramac Configurable Compute Engine," Field Programmable Logic and Applications, 5 <sup>th</sup> International Workshop, FPL '95 Oxford, United Kingdom, pp. 44-53.
	XILINX, "The Programmable Gate Array Design Handbook," First Edition, 1986, pp. i-A-10.

EXAMINER 	DATE CONSIDERED 3/30/04
EXAMINER: Initial citation if reference was considered. Draw line through citation if not in conformance to MPEP 609 and not considered. Include copy of this form with next communication to applicant.	